1. Do question 3.5 (chapter 3). This question can be seen in the attachment with the submission link for HW4. Please note that if your Boolean equation or gate-level design itself is not 100% correct then that will not make you lose marks. The purpose here is to familiarize you with the different ways you can represent a digital design in VHDL. When actually designing a circuit/system you will select the best way yourself. In this type of problem, that will be through if-then-else or when-else statement, but this problem asks for more just to show you other possibilities in VHDL.

Text

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**If-then-else**

Graphical user interface, application

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**Boolean**

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**When-else**

**Text

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**Component Instantiation**

**Graphical user interface, text

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